in a normal read to difference the high or "1" states, having a threshold level above $V_R$, from the low or "0" states, having a threshold level below $V_R$. This is described, for example, at page 19, lines 21-23.

The lowest of the levels in Figure 10, $V_E$, is used during the erase process to verify that the cells to be erased are sufficiently erased. The used of this distinct $V_E$ value results in the cells to be erased are erased by the margin ($V_R$-$V_E$) below the normal read level $V_R$. This process is described generally on page 20, lines 6-14, and in more detail with respect to Figure 7 between page 22, line 11, and page 23, line 5. As shown in Figure 7, this process consists of the erasing the cells (701), reading the cells with their control gates at $V_E$ (702), and repeating the process (703) until the cells verify as being in a "0" state by having a threshold value $V_{th} \leq V_E < V_R$.

The highest of the levels in Figure 10, $V_{PV}$, is used in a similar fashion during the program process to verify that the cells to be programmed to a "1" state are sufficiently programmed. The used of this distinct $V_{PV}$ value results in the cells to be programmed being programmed above the normal read level $V_R$ by the margin ($V_{PV}$-$V_R$). This process is described generally from page 19, line 28, to line 5 of page 20, and in more detail with respect to Figure 8 between page 23, line 6, and page 24, line 4. As shown in Figure 8, this process consists of the writing data to the cells (801), reading the cells with their control gates at $V_{PV}$ (802) to verify whether they are successfully written to the "1" state, and repeating the process (803) until the cells verify as being in a "1" state by having a threshold value $V_{th} \geq V_{PV} > V_R$.

The programming process shown in Figure 8 also employs two other voltages levels, Program Read High $V_{PRH}$ and Program Read Low $V_{PRL}$, for the purpose of read "0" and "1" margining, as described generally on page 20, lines 15-26. The purpose of this process is to check that, after a programming process (using $V_{PV}$) is completed, that the "0" states and "1" states are still, in fact, in the states "0" and "1" with sufficient margin. The "0" or low states are checked by a read using a level $V_{PRL}$ below the normal read level $V_R$, but less stringent than the erase verify level $V_E$: $V_E < V_{PRL} < V_R$. Similarly, the "1" states are checked by a read using a level $V_{PRH}$ above the normal read level $V_R$, but less stringent than the program verify level $V_{PV}$: $V_{PV} > V_{PRH} > V_R$. This read margining process occurs in steps 804-807 of Figure 8 and is described on page 24, lines 5-20.

(Concerning the terminology "Program Read Low", it should be noted that the Program Read Low level, $V_{PRL}$, is used to check the low or "0" level, but that this is done as part of the program process in steps 806 and 807. It is not used to check a "programmed" or "1" state: that is, it is used to read the low level as part of the programming algorithm of Figure 8, not as an additional, lower read level for the "programmed" or "1" states.)

The last pair of levels in Figure 10 are what are referred to in the application as the "scrub" values, the purpose of which is described generally from page 20, line 27, to page 21, line 22. As described there, this process is used to check whether the threshold of any of the memory cells have drifted during the operation of the memory sufficiently close to the normal read level so that an error may result eventually when the data of these cells is read. The low or "0" are checked in this process using the Scrub Low level $V_{SL}$ and the high or "1" levels are checked using the Scrub High level $V_{SH}$ in the process of Figure 9. As shown in Figure 10, the scrub high value $V_{SH}$ is above the normal read level $V_R$, but below the program verify level $V_{PV}$ used when the cells are programmed to the "1" state: $V_R<V_{SH}<V_{PV}$. Similarly, the scrub low value is intermediate to the normal read level and the erase verify level: $V_R>V_{SL}>V_E$.

The scrub process of Figure 9 is described between page 24, line 27, and page 26, line 3. This process determines whether memory cells have a threshold level below the Scrub High level $V_{SH}$ (901 and 902) and above the Scrub Low level $V_{SL}$ (903 and 904). As described from page 20, line 27, to page 21, line 22, if a cell has a threshold value between these scrub values, $V_{SL}<V_{th}<V_{SH}$, it is considered to have too little margin to the normal read value $V_R$ and to be a soft error. This corresponds to the "NO" paths, leading to step 905, where the cell is reprogrammed. "The steps of this program operation follows the procedure set forth in Fig. 8" (p. 20, lns. 20-22), where, as described above, the cell is programmed until it is above the Program Verify level $V_{PV}$.

The pending claims are drawn to the scrub process of Figure 9. As described, this process consists of determining that a cell has a level in the range between the low and high scrub values; that is, above $V_{SL}$ and below $V_{SH}$. As can be seen from Figure 10, it is therefore also above the erase verify level $V_E$, which is used to determine that a cell is properly erased, and below the program verify level $V_{PV}$, which is used to determine that a cell is properly programmed. If the cell falls into this range, it is then programmed according to the process

of Figure 8, so that it above the program verify level $V_{PV}$. As $V_{PV}>V_{SH}$, it is also programmed to above $V_{SH}$.

It is respectfully submitted that this is the process as described in the all of the pending independent claims. The claims are written in terms of "a charge level"; however, as noted beginning on page 2, line 17, of the application, a cell's threshold level is a function of its charge level. Consequently, it is believed that adequate support is presented in the application for all of the pending claims.

Claims 37 and 39

Specifically, claim 37 is written in terms of the erase verify level $V_E$ and the programmed verify level $V_{PV}$:

> 37. A method of improving data retention in a nonvolatile writeable memory having an erased-cell reference level and a programmed-cell reference level, the nonvolatile writeable memory having a plurality of memory cells, each of the memory cells being in an erased state when storing a charge below the erased-cell reference level [$V_E$], and each of the memory cells being in a programmed state when storing a charge above the programmed-cell reference level [$V_{PV}$], the method comprising the steps of:
>
> (a) identifying a memory cell having a charge above the erased-cell reference level [$V_E$] and below the programmed-cell reference level [$V_{PV}$]; and
>
> (b) programming the memory cell until the charge of the memory cell is above the programmed-cell reference level [$V_{PV}$].

The voltage levels have been added in braces to the claim for clarity. As noted above, the process of Figure 9 actually determines that the cell is above the level $V_{SL}$ and below $V_{SH}$; but as $V_{SL}>V_E$ it is also above $V_E$; and as $V_{SH}<V_{PV}$, it is also below $V_{PV}$. Consequently, it is respectfully submitted that a rejection of claim 37 under 35 U.S.C. 112, first paragraph, is not well-founded and should be withdrawn as support for element (b) of claim 37 is contained in step 905 of Figure 9 and the program process of Figure 8.

The support for claim 39 is the same as that for claim 37. Claim 39 differs in that it is written in terms of a first and a second threshold level instead of an erased-cell reference level and a programmed cell reference level. The first and second levels can be taken as $V_{SL}$ and $V_{SH}$, respectively. With the corresponding levels included in brackets, claim 39 reads:

> 39. A method of improving data retention within a non-volatile writeable memory, the method comprising the steps of:
>
> (a) identifying a group of one or more memory cells having a stored charge over a first threshold [$V_{SL}$] and less than a second threshold [$V_{SH}$]; and
>
> (b) programming each memory cell of the group of one or more cells until each of the memory cells has a stored charge over the second threshold [$V_{SH}$].

As described above, the cells are programmed until they are greater than the level $V_{PV}$; but as $V_{PV}>V_{SH}$ , they are also greater than $V_{SH}$. Consequently, it is respectfully submitted that a rejection of claim 39 under 35 U.S.C. 112, first paragraph, is not well-founded and should be withdrawn as support for element (b) of claim 39 is contained in step 905 of Figure 9 and the program process of Figure 8.

(It should be noted that these claims have been described in the simplest form with respect to the various levels shown in Figure 10 and how these levels are used in Figures 8 and 9. However, they are also supported using the various sets of voltage levels other than described above. This follows due to the relations that $V_{PV}>V_{PRH}>V_{SL}>V_R$ and that $V_R>V_{SL}>V_{PRL}>V_E$. Thus, for example, both of claims 37 and 39 are also supported in terms of the pair $V_{SL}$ and $V_{SH}$. To keep the explanations simpler, and since support is only needed in terms of one set parameters, the other variations will not be discussed further at present. This is also true of claims 42 and 46 below.)

Claims 42 and 46

Claims 42 and 46 differ from claims 37 and 39 in that they contain an initial step of either writing data or accessing the sector of cells. This corresponds to occurrence of the scrub process as step 808 in Figure 8, where the earlier steps in Figure 8 have accessed a sector of cells in order to program them. Alternately, a sector may also be accessed for a read process prior to the scrub, as described at page 25, line 27, to page 26, line 3. In claims 42 and 46, the Office Action fails to find support for the identifying step. It is respectfully submitted that these claims also are supported in the present application as generally described above. As with claim 39, the description here is again given using the low scrub level $V_{SL}$ and the high scrub level $V_{SH}$.

In the binary embodiment of the present invention, the "0" state and the "1" state are determined based on whether their level is respectively below or above the normal read $V_R$ of Figure 10. If a cell has a level below the scrub level $V_{SL}$, it is also below $V_R$ (as $V_{SL}<V_R$) and therefore in the "0" state. Similarly, if a cell has a level above the scrub level $V_{SH}$, it is also above $V_R$ (as $V_{SH}>V_R$) and therefore in the "1" state. As in claim 39, the support for claims 42 and 46 is given in terms of $V_{SL}$ and $V_{SH}$.

With references to the states and the reference levels included in brackets, claim 42 reads:

42. A method of improving data retention in a nonvolatile writable memory having a first reference level [$V_{SL}$] and a second reference level [$V_{SH}$], the nonvolatile writable memory having a plurality of memory cells, each of the memory cells being in an first state ["0"] when storing a charge below the first reference level [$V_{SL}$], and each of the memory cells being in a second state ["1"] when storing a charge above the second reference level [$V_{SH}$], the method comprising:

writing into each of a set of the plurality of memory cells a respective data value, wherein the data values are one of the first ["0"] and second ["1"] states;

identifying a memory cell of the set having a charge above the first reference level [$V_{SL}$] and below the second reference level [$V_{SH}$]; and

rewriting the respective data value into the memory cell.

As described above, the process of Figure 9 corresponds to determining that a memory cell has a level below $V_{SL}$, here the second reference level, and above $V_{SH}$, here the second reference level. Consequently, it is respectfully submitted that a rejection of claim 42 under 35 U.S.C. 112, first paragraph, is not well-founded and should be withdrawn as support for the second step of claim 42 is contained in steps 901-904 of Figure 9 as described beginning on line 27 of page 24.

Similarly, it is also respectfully submitted that support is provided for the identifying step of claim 46 and that a rejection of claim 46 under 35 U.S.C. 112, first paragraph, is also not well-founded and should be withdrawn as support for the second step of claim 42 is contained in steps 901-904 of Figure 9 and its corresponding description.

Conclusion

Therefore, it is respectfully submitted that the present application fully supports the claimed subject matter and that a rejection under 35 U.S.C. 112, first paragraph, is not well founded, and that claims 37 and 39-50 are allowable. Reconsideration of the Office Action's rejection of claims 37 and 39-50 is respectfully requested. If the Examiner has any question concerning the support for the pending claims, a call to the undersigned is invited.

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Respectfully submitted,

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